

REMARKS

Applicants respectfully request further examination and reconsideration in view of the following remarks. Claims 15-30 remain pending in the case. Claims 15-30 are rejected.

35 U.S.C. §102(b)

Claims 15-18, 21, 22 and 26-30 are rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent 5,879,990 by Dormans, et al., hereinafter the "Dormans" reference. Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as recited in Claims 15-18, 21, 22 and 26-30 are not anticipated by Dormans.

Independent Claim 16 recites (emphasis added):

A process of fabricating a memory cell comprising a substrate that comprises a first region and a second region with a channel therebetween, the method comprising:

forming a gate above said channel of said substrate,
wherein said gate comprises a single polysilicon layer;
forming bitlines on both sides of said gate subsequent to
said forming said gate comprising said single polysilicon layer;
and
siliciding said bitlines.

Claims 15, 17, 18, 21, 22 and 26-30 that depend from independent Claim 16 provide further recitations of the limitations of the present invention as claimed.

Applicants understand Dormans to teach a semiconductor device having an embedded non-volatile memory. Dormans does not teach, show or suggest fabricating a memory cell, as claimed. Specifically, Applicants respectfully submit that Dormans teaches a non-volatile memory cell having at least two poly layers. Applicants respectfully assert that, Dormans does not show or suggest a process of fabricating a memory cell comprising “forming a gate above said channel of said substrate, wherein said gate comprises a single polysilicon layer,” as claimed (emphasis added).

Examiner cites gate 22 of Dormans as including a single polysilicon layer. However, Applicants respectfully assert that Dormans does not teach that gate 22 includes a single polysilicon layer, but rather includes a double polysilicon layer. With reference to Figure 1 of Dormans, a first polysilicon layer 7, poly A, is deposited (col. 3, lines 65-67). With reference to Figure 5 of Dormans, a third poly layer 19, poly C, is deposited on first poly layer A (col. 4, lines 53-61). A photomask is provided and, as shown at Figure 6, the non-masked poly is etched away to obtain gate 22. Specifically, gate 22 includes both poly A and poly C, and therefore includes a double polysilicon layer.

In contrast, the claimed invention is directed to a process of fabricating a memory cell comprising “forming a gate above said channel of said substrate, wherein said gate comprises a single polysilicon layer” (emphasis added). As described in the present specification in accordance with Figure 2, a polysilicon

1 layer 311 is deposited on ONO layer 302. In particular, poly 1 layer 311 is the only poly layer of gate, and is therefore includes a single polysilicon layer.

Moreover, Applicants respectfully assert that Dormans does not teach, describe or suggest a memory cell including a bitline. Applicants respectfully assert that, Dormans does not show or suggest a process of fabricating a memory cell comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said single polysilicon layer,” as claimed (emphasis added). Examiner cites source and drain zones 24 and 25 of Dormans as being bitlines. Applicants respectfully assert that source and drain zones 24 and 25 are bitlines. In particular, Dormans is silent as to the use of a bitline.

Applicants respectfully assert that nowhere does Dormans teach, disclose or suggest a memory cell comprising “forming a gate above said channel of said substrate, wherein said gate comprises a single polysilicon layer” and “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said single polysilicon layer” (emphasis added) as recited in independent Claim 16, that this claim overcomes the Examiner’s basis for rejection under 35 U.S.C. § 102(b), and is thus in a condition for allowance. Therefore, Applicants respectfully submit that Dormans also does not show or suggest the additional claimed features of the present invention as recited in Claims 15, 17, 18, 21, 22 and 26-30 that depend from independent

Claim 16. Therefore, Applicants respectfully submit that Claims 15, 17, 18, 21, 22 and 26-30 overcome the Examiner's basis for rejection under 35 U.S.C. § 102(b) as these claims are dependent on an allowable base claim.

35 U.S.C. §103(a)

Claims 19, 20 and 23-25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dormans in view of United States Patent 6,218,695 by Nachumovsky, hereinafter the "Nachumovsky" reference. Claims 19, 20 and 23-25 depend from independent Claim 16. Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention as recited in Claims 19, 20 and 23-25 is not unpatentable over Dormans in view of Nachumovsky.

As described above, Applicants understand Dormans teaches a non-volatile memory cell having at least two poly layers. Applicants respectfully assert that, Dormans does not show or suggest a process of fabricating a memory cell comprising "forming a gate above said channel of said substrate, wherein said gate comprises a single polysilicon layer," as claimed (emphasis added). In particular, by teaching a non-volatile memory cell having a double poly layer, Dormans teaches away from a non-volatile memory cell including a single poly layer, as claimed.

Moreover, Applicants respectfully assert that Dormans does not teach, describe or suggest a memory cell including a bitline. Applicants respectfully assert that, Dormans does not show or suggest a process of fabricating a memory cell comprising “forming bitlines on both sides of said gate subsequent to said forming said gate comprising said single polysilicon layer,” as claimed (emphasis added). Examiner cites source and drain zones 24 and 25 of Dormans as being bitlines. Applicants respectfully assert that source and drain zones 24 and 25 are bitlines. In particular, Dormans is silent as to the use of a bitline.

Furthermore, the combination of Dormans and Nachumovsky fails to teach or suggest the claim limitation of a memory cell comprising “forming a gate above said channel of said substrate, wherein said gate comprises a single polysilicon layer” (emphasis added) because Nachumovsky does not overcome the shortcomings of Dormans. Nachumovsky, alone or in combination Dormans, does not show or suggest a process of fabricating a memory cell comprising “forming a gate above said channel of said substrate, wherein said gate comprises a single polysilicon layer,” as claimed.

Applicants understand Nachumovsky to teach area efficient column select circuitry. In particular, Nachumovsky is silent as to how the memory cells of the circuitry are fabricated. In particular, Nachumovsky does not teach, describe or suggest a process for fabricating a memory cell including “forming

a gate above said channel of said substrate, wherein said gate comprises a single polysilicon layer" (emphasis added).

Applicants respectfully assert that nowhere does the combination of Dormans and Nachumovsky teach, disclose or suggest the present invention as recited in independent Claim 16, that this claim overcomes the Examiner's basis for rejection under 35 U.S.C. § 103(a), and is thus in a condition for allowance. Therefore, Applicants respectfully submit that the combination of Dormans and Nachumovsky also does not show or suggest the additional claimed features of the present invention as recited in Claims 19, 20 and 23-25 which depend from independent Claim 16. Therefore, Applicants respectfully submit that Claims 19, 20 and 23-25 overcome the Examiner's basis for rejection under 35 U.S.C. § 103(a) as this claim is dependent on an allowable base claim.

CONCLUSION

Based on the arguments presented above, Applicants respectfully assert that Claims 15-30 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge our deposit account No. 23-0085 for any unpaid fees.

Respectfully submitted,
WAGNER, MURABITO & HAO L.L.P.

Dated: 20 June, 2005

A handwritten signature in black ink, appearing to read 'Matthew J. Blecher', written over a horizontal line.

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